International Journal of Current Research and Applied Studies, (IJCRAS)

ISSN: 2583-6781

available at https://ijcras.com/

Volume 1 Issue 3 July-August 2022

Page 35-54

ENHANCED QUANTUM EFFICIENCY POROUS SILICON BASED PHOTOVOLTAIC SOLAR CELL

Bello Hamza Abdullahi[1], Jamilu Tijjani Baraya[2] and *Nura Muhammad Shehu[3]

[1,2]Department of Physics, Federal University Dutsin-Ma, Katsina State, Nigeria.

[3]Department of Physics, Bayero University, Kano, Kano State, Nigeria.

ABSTRACT

The quantum efficiency of crystal silicon (i.e photosensitive device) is enhanced by making it porous so that it absorbs most of the photons falling on its surface in order to produce charge carriers, and as a result of this stage a heterojunction is as well formed. The porous side is doped with an impurity which is different from that of the wafer impurity used to form P-N junction, at last two contacts are taken from the porous side and the back side, gold and silver respectively to form ohmic and schottky junction which also contributed to achieve the final goal.

Keywords: Heterojunction, Optical Quantum Efficiency, P-N Junction, Porous.

1. INTRODUCTION

In the Era of high technology and diversified electronics world, electronics plays a very important role in the human development through different aspects. Though a lot of challenges were faced by the engineers and researchers on how they can make the resources available, so as to make good use of them. Because of their scarcity, sometimes some alternatives have to be taken in order to provide those resources available. For these and other reasons, it becomes necessary to study matter from its micro and nano levels so as to alter some of its properties to suit the needs. All materials have differences in properties between their nano, micro and bulk state. Electronics components are the back bone of the entire circuits developed in the world, because all of them were developed from those components. Therefore, there is a

need to make different studies in order to obtain such components using different method, different materials but with high efficiency [1]. Moreover, many efforts were made by different scientists so far, concerning porous silicon, which is the main topic in this research, but in history porous silicon was discovered by a scientist called uhlir, accidently while performing electro-polishing experiments on silicon wafers using an electrolyte containing hydrofluoric acid [2]. Its development was first justified for technological reasons, in particular, localized isolation in microelectronics. A renewed interest in porous silicon occurred in 1990 when its photoluminescence and electroluminescence properties were demonstrated [3]. This doesn't stop at that, there are many more discoveries about such material across the world because of its importance especially in this field. Presently many electronic devices are fabricated using high efficient materials like gallium arsenide example optical devices like light emitting diode (LED) and much more. Though silicon is cheaper than above mentioned gallium arsenide, it can serve same purpose but only if its quantum efficiency is enhanced so that it provides enough photon to charge carrier ratio that can serve the aim [4]. Now, this research will focus on enhancing quantum efficiency of silicon by improving the photon absorption of the material, due to its refractive index (about 3.5) it reflects major part of the photon instead of absorbing and provides hole-electron pair which can serve our purpose [3].

1.1 Quantum efficiency (QE)

The quantum efficiency (QE), of photosensitive devices (i.e any device that produce charge when light falls on it) is the percentage of photons hitting the surface that produce charge carriers (i.e Photoluminescence) [5]. It is measured in electrons per photon or amps per watt. QE of a solar cell is a measurement of a charge carries produced by the solar cells when light excited on it. Since the energy of a photon is inversely proportional to its wavelength, QE is often measured over a range of different wavelengths to characterize it's efficiency at each photon energy level. The QE for photons with energy below the band gap is zero. Literally, band gap is the separation or distance between the top of the valence and bottom of the conduction bands [6]. For an electron to transited from one band to another, it has to have an energy equal to at least the energy between the gap which is called band gap energy [7].

1.2 Types of Quantum Efficiency

(a) *External Quantum Efficiency* (EQE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy shining on the solar cell from outside (incident photons) [2].

(b) *Internal Quantum Efficiency* (IQE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy that shine on the solar cell from outside and are absorbed by the cell [2]. In general, the IQE is mostly larger than the EQE. A low IQE indicates that the active layer of the solar cell is unable to make good use of the photons. For the measurement of IQE, EQE of the solar device has to be measured first, then measures its transmission and reflection, and combines these

data to infer the IQE.

$$\text{EQE} = \left(\frac{\frac{electrons}{sec}}{photons/sec}\right) = \left(\frac{current/(charge\ of\ 1\ electron)}{(total\ power\ of\ photons)/(energy\ of\ 1\ photon)}\right) \quad (1)$$

The external quantum efficiency therefore depends on the two phenomena; absorption of light and the collection of charges. The photon is being absorbed and then generates an electron-hole pair; these charges are separated and collected at the junction. A "good" material avoids charge recombination which causes a drop in the external quantum efficiency [2]. The ideal quantum efficiency graph has a square shape, where the QE value is fairly constant across the entire spectrum of wavelengths measured. However, due to the effects of recombination the QE for most solar cells is reduced, where charge carriers are not able to move into an external circuit [8]. The same mechanisms that affect the collection probability also affects the QE. For example, modifying the front surface can affect carriers generated near the surface. And because high-energy (blue) light is absorbed very close to the surface, considerable recombination at the front surface will affect the "blue" portion of the QE. Similarly, lower energy (green) light is absorbed in the bulk of a solar cell, and a low diffusion length will affect the collection probability from the solar cell bulk, reducing the QE in the green portion of the spectrum [9]. Generally, solar cells on the market today do not produce much electricity from ultraviolet and infrared light ($< 400\,nm$ and $> 1100\,nm$ wave lengths, respectively); this light is either filtered out or absorbed by the cell, heating the cell [4].

Therefore, this study will make the solar cells more efficient and reduce the losses from the effects discussed so far. It's very important to consider the cost, and the resources utilize during energy production, for that, to improve the quantum efficiency is a very important way to conserve resources as well as the effort towards this application [10].

1.3 Antireflection Coating (ARC)

From our discussion so far, we understood one of the effects that decreases the quantum efficiency of silicon, because of the refractive index between air and the silicon surface which entirely reduces the absorption of the photons by the surface [11]. Though different approaches were used by scientists, the problem was the alternative method they took it either reduces the conductivity of the material or increases the resistivity which also alters the quantum efficiency. Therefore, by borrowing the technique that has been well developed in optical science, producing a porous on the silicon surface will reduce such reflection and serve as ARC [12]. Basically, this technique used Bragg reflection phenomenon that is an interference effect caused by thin film structure. The reflectance occurs when the light incidence on an interface of two material with different index of refraction $n_1 \neq n_2$ [3]. This study is necessary due to high demand of highly efficient solar cells to help in producing high renewable energy using minimum resources. Moreover, in other electronics fields such efficiencies will help in developing small components such as photo detectors, LEDs, etc.

2. GENERAL METHODOLOGY

2.1 Materials and Procedure

The wafers used are N-type and P-type silicon of different orientation (111) N-type, (100) N-type and (100) P-type. All the three wafers mention are high resistive 1- 5 Ωcm², 1-5 Ωcm² and 1-10 Ωcm² respectively. There are two conditions involved, electrochemical etching (ECE) and photo-electrochemical etching (PECE) which involve the use of light. The average temperature in the room where the experiment took place was 20℃. Initially, the wafers were prepared by cutting them in sizes that can fit in the double cell. Then the wafers were clean to remove any traces of dust, oil or finger print that may alter the resulting structure formed. The cleaning process used was standard RCA (named after Radio Corporation of America) clean studied by Werner Kern which involve the following steps. The RCA clean is known as a front end of line FEOL clean. The original RCA clean sequence is:

i. Standard Clean 1 (SC1) - 5 volumes of H_2O, 1 volume of hydrogen peroxide (H_2O_2).
ii. 30% 1 volume of ammonium hydroxide (NH_4OH), 29% was heated at $70 - 80$℃.
iii. Ultrapure water rinsed.
iv. Standard Clean 2 (SC2) - 6 volumes of H_2O, 1 volume of H_2O_2 and 30% 1 volume of Hydrochloric acid (HCl), 27% was heated at 70℃.
v. Ultrapure water rinsed and dried.
vi. The SC1 clean takes out organic residues and particles. The SC1 clean works by creating and dissolving hydrous oxide films. The SC2 clean takes alkali metal and hydroxides - Li, Al, Ti, Zn, Cr, Fe, Ag, Pd, Au, S, Cu, Ni, Co, Pd, Mg, Nb, Te, W, Na, Fe (leaves Cl Residues) out. The second method used is:
vii. Sulfuric Peroxide (SPM) - 4 volumes of sulfuric acid (H_2SO_4) 98%, 1 volume of H_2O, 30% at 130℃ for 10 to 15 minutes.
viii. Ultrapure water rinsed.
ix. Dilute hydrofluoric acid (DHF) - 50 volumes of H_2O, 1 volume of hydrofluoric acid (HF), 49% at room temperature for 10 seconds.
x. Ultrapure water rinsed.
xi. SC1 for 20 minutes.
xii. Ultrapure water rinsed.
xiii. SC2 for 15 minutes.
xiv. Ultrapure water rinsed and dried.

The SPM makes the bulk organic removal and chemically oxidized the wafer surface in the anteceding sequence, the DHF removes the chemical oxide, SC1 removed particles and SC2 removed metals. Furthermore, the silicon wafers dried using nitrogen gas before the etching process. The electrochemical process used is called anodization process. In this process the cell used is a double tank cell. So that the wafer was inserted in between the half cells. And the half cells were linked through a small circle through which the conduction takes place from one half cell through the chemical via the wafer (i.e through the small circle that link the half cells) to the other half cell. The area of the silicon that is within the circle

was the etching site of the wafer, because is the only part that have a contact with the HF. There are two platinum electrodes, one in each of the half cell. These electrodes are used because they are HF resistance and conductive. The HF concentration can be obtained by considering the application in hand (i.e wafer properties). The HF concentration is formed from the portion of the HF and surfactant in a certain proportion, in this work ethanol was used as surfactant with a percentage of 99.2% and the HF used is 40%. The concentration was selected from the suitable concentrations used by other literatures that wrote about solar applications using porous silicon. İn most of those literatures the concentration is 10%, but this concentration depends on the available chemicals in hand, because the concentration of the available chemicals determines the proportion. It can be calculated as follows:

To obtain a certain percentage we have;

$$\frac{\boldsymbol{a}\times\boldsymbol{b}}{\boldsymbol{a}+\boldsymbol{c}} = \boldsymbol{d}\% \qquad (2)$$

Where
a = HF proportion used
b = HF concentration available
c = ethanol proportion needed
d = the percentage concentration suitable for the application in hand.

Therefore, let take $a = 1$, $b = 40\%$, and $d = 10\%$ to find c, we have:

$$\frac{1 \times 40}{1 + c} = 10$$

$$\Rightarrow c = \frac{40 - 10}{10}$$

$$c = 3\ portion \qquad .(3)$$

Therefore, the 10% obtained comprised of 3 portion of ethanol 96% and 1 portion of HF 40% (i.e 3:1). This concentration is suitable for high resistive wafers, because the impurities are less, therefore the fluorine ion can reach the silicon easily and etch it away. But in contrary, low resistive wafers have different case, since the impurities are high, they can block the access to the silicon, therefore more HF concentration will be suitable for it.

2.2 Methods Involved

a. Anodization Process

This experiment took place under fluorescent light at a temperature of 20℃ with a double tank cell. This cell is an open cell without stirrer. Power supply is used to generate the current through the electrolyte, and to obtain the precise current density needed, and ammeter was used in series with the power supply so that the measurement is precise. The cell comprises of two separate chambers, where by, they stacked together by the used of bold and nut after placing the sample in between them. Certain precautions were

taken before the beginning of the experiment, because it involves dangerous chemicals such as hydrofluoric acid. After the solution is prepared then the power generator is set to specification, the specification were:

The cell is filling up with the solution and then the platinum electrode were placed and crocodile jumpers are used to connect from the generator to the electrodes. Normally, the negative terminal is placed on the face that the porous is willing to developed, and same is done here. The electric circuit is developed and current passed through the wafer via the solution in the adjacent cells. As a result, one face is etched and produced some porous layer. All the samples are fabricated the same way, though the result may vary, due to anodization parameters used, but in all cases the porous is formed as described. There are nine samples obtained in all, three each from one type of silicon wafer as mentioned earlier. The samples prepared are as follows:

i. Single Layer Porous Silicon

This was prepared with only single layer on the substrate (i.e same condition is used for the whole process). For this set of samples, the current density used is 20 mA/cm² with solution concentration (i.e HF concentration) 10% at the duration of 20 minutes. In the case of N-type porous, illumination is needed, and this was done using a table lamp in all cases.

ii. Multilayered One

This was prepared with double layered porous on the substrate (i.e different conditions were used for each layer). In the first layer, the current density is 50 mA/cm² in a solution concentration of 10% at the duration of 10 minutes, then suddenly the current was changed to 30 mA/cm² but the remaining parameters remain the same until next 10 minutes. In all, the process takes 20 minutes from it starts.

iii. Multilayered Two

This is also double layered porous, in the first layer, the current density used is 30 mA/cm² in a solution of 10% at duration of 10 minutes. The second layer has current density of 20 mA/cm² with same condition as the first layer only the current density changes. In all the time duration was 20 minutes, 10 minutes for each layer.

b. Drying of Porous Silicon

The drying of porous silicon is done by a method explained below;

i. Drying with Nitrogen gas

The magnitude and effects of the capillary stresses has been reduced (but not eliminated) by the method used in the drying of the sample (i.e porous layer produced), therefore nitrogen was used to dry the porous silicon so that the structure will not be damage by cracks.

ii. Doping

P-N junction is formed by doping N-type substrate at the porous site with P-type doping (i.e boron) likewise P-type substrate is doped with N-type at the porous site, hence the P-N junction is formed.The

method used in both cases to dope the impurities will be explained as follows;

iii. Doping N substrate with P impurities

In this case, thin layer impurity is deposited on the porous site using sputtering in which a little portion penetrate through the nano wires porous while some remain at the surface. Later they are diffused to the silicon by annealing at a temperature of 900°C. This temperature is used knowing the melting temperature of silicon which is 1400°C, therefore it will not melt and it will be suitable for the purpose.

iv. Doping P substrate with N impurities

This was done using chemical method. It involves combining one portion of $POCl_3$ to five portion of acetone, then the solution is doped in the porous site and penetrate through the pores then dry, for uniformity, the solution is drop on the porous while its spinning on spinner. It was also annealed at 700°C using furnace.

c. RF and DC Magnetron Sputtering Deposition

Aluminium film was deposited using this method. Ar+ ions formed in a plasma are accelerated towards a target material (i.e Aluminium target). These high energy ions eject some amount of target material atoms. Then these atoms were transported to the substrate in vacuum. Since target atoms were not evaporated there is no need for high temperatures hence there are no hot parts in a sputtering system. Materials that cannot be deposited in an evaporator due to their high melting point can easily be deposited in a sputtering system.

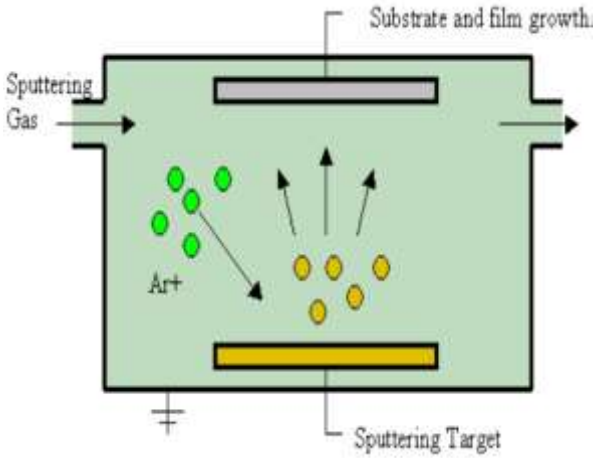


Figure 1: Description of RF and DC Magnetron Sputtering Deposition

Figure 2: RF and DC Magnetron Sputtering Deposition, photo taken from BioNano Technology Research and Development Center, Fatih University, Istanbul, Turkey.

d. Electron Beam Deposition

The deposition of Gold film was carried out using this method. In this system, the target material is bombarded by a high energy electron beam. The arising heat energy evaporates the target material. The vapor from target material deposits on the substrate. By this technique, single crystal films at relevant growth conditions, amorphous thin films and many other structures can be growth on the substrate surfaces in a varying thickness and dimension from nanometer to micrometer scale. But in this case the gold film was deposited using this method.

2.3 MEASUREMENTS

We need to explain briefly how the contacts were taken before the measurements were obtained from the fabricated samples. This has significant effects on the result, because bad contacts might give failed results even if all the steps were right. After the methods described above, a copper wire of approximately 0.2 mm in radius was use along with a silver paste to take the contact from both side of the wafer. The picture of the sample is shown in figure 3 below.

As shown in figure 3, three contacts were taken. At the porous point one contact is taken as the positive potential, and at same porous side but the crystalline part another contact was taken, then the last contact from the back side of the sample.

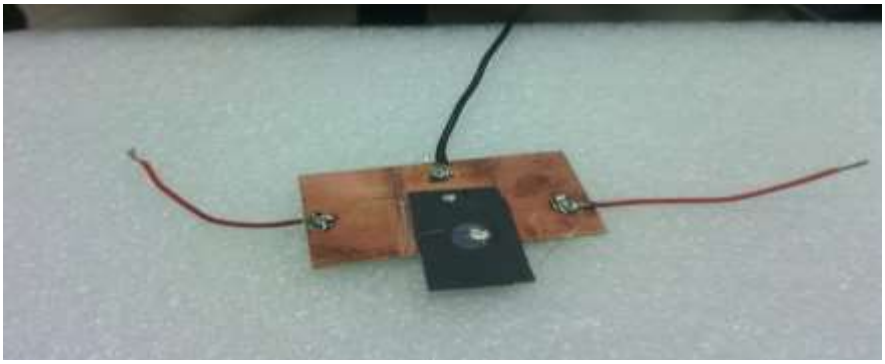


Figure 3. Picture of the sample produced with contacts.

The instruments employed for the measurements in this research are Confocal Microscope (CSLM), Semiconductor Characterization System, Scanning Electron Microscope, and method of Current-Voltage measurement of a solar cell where the instruments involved are solar cell module, ammeter, voltmeter, variable resistor, alligator clips and jumpers and light source. These instruments are available at the BioNano Technology Research and Development Center, Fatih University where the experiment was conducted.

Figure 4: Structure of Confocal Microscope, photo taken from BioNano Technology Research and Development Center, Fatih University, Istanbul, Turkey.

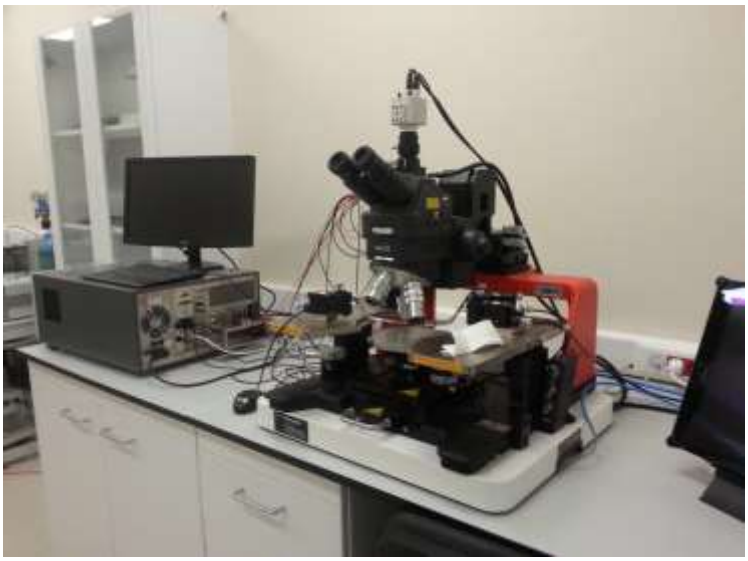


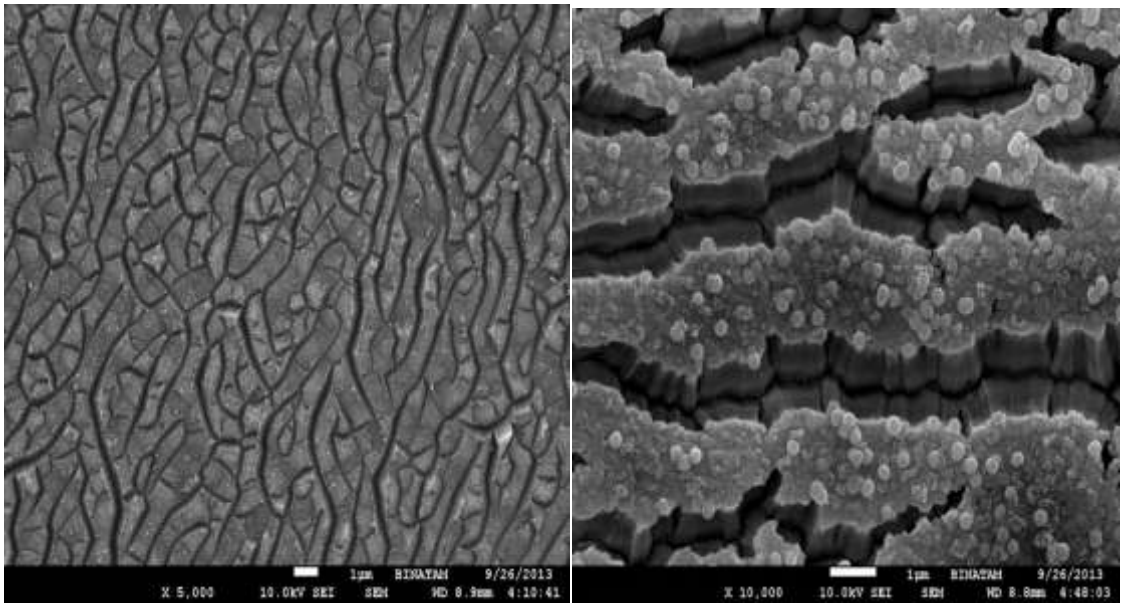
Figure 5: Semiconductor Characterization System, photo taken from BioNano Technology Research and Development Center, Fatih University, Istanbul, Turkey.

Figure 6: Scanning Electron Microscope, photo taken from BioNano Technology Research and Development Center, Fatih University, Istanbul, Turkey.

3. RESULTS AND DISCUSSION

All the samples were prepared using same methods (anodization method) but different parameters, but they have same effect toward the efficiency. Therefore, the sample with the highest output shall be used to compare against the non-etched silicon wafer from which the sample was prepare to see how much the efficiency is improving. In addition to that, we can take some of the measurement against standard existing

solar cells and see which effect can be observed from the fabricated one. The set of samples used in the work are P (100) high resistive with resistivity of 10 Ωcm, N (100) high resistive and N (111) high resistive with the resistivity of 1 Ωcm. In all cases, three different set of samples were prepared single layered porous using anodization process with the current density of 20 mA/cm², solution concentration (HF: ethanol) 10% and anodization time 20 minutes. These specifications were used for all the three samples to obtained single layered porous for each of the samples. The second sample is multilayered porous using same method but with the specification's current density one (j_1) 50 mA/cm², current density two (j_2) 30 mA/cm², solution concentration (HF: ethanol) is 10% and the time is 20 minutes for each layer. Same as in the first case these conditions are used for all the three samples. Then the last set of samples were prepared using the same method but different specifications, this is also multilayered with current density one (j_1) 30mA/ cm², current density two (j_2) 20 mA/cm², solution concentration (HF: ethanol) is 10% and the time is 20 minutes for each layer. Until now, nine samples were prepared three set per each specification, all the specifications were obtained from the past literatures that study on solar cells efficiency, the optimized values where used so that to observed the effect on the efficiency of the prepared sample. The Scanning Electron Microscope SEM image obtained for the samples is shown in figure 7.



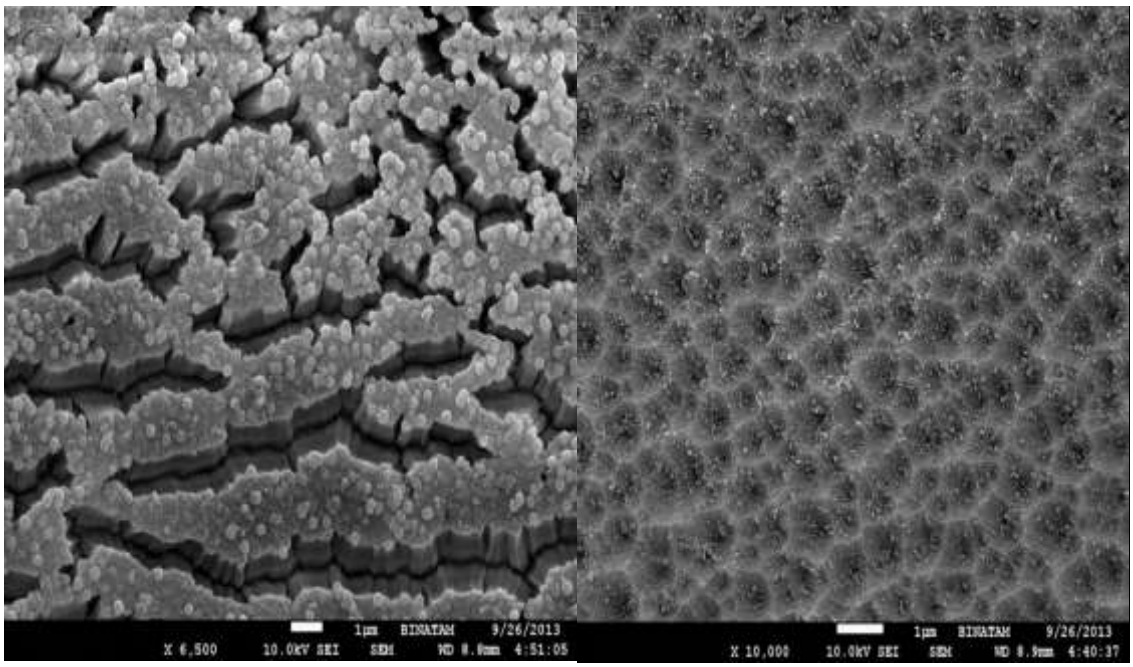


Figure 7: SEM images of the porous samples

As shown in figure 3, the surface of the c-Si sample was completely etched and consisted of numerous tiny pores formed over the soft wall. The formation of numerous new tiny pores inside the initial pores can be distinguished clearly. These pores results from the conditions used in the fabrication, double pores for multilayer and single pore for the single layer is clearly observed in the SEM image. The approximate pore size obtained is in the range of few Nano-meters scale, these range is the suitable range for solar cells. There are highly dense pores on the surface which is also important for manipulating the surface to obtain the suitable way of improving absorption on the surface. The porosity is high up to around 90% obtained from the following formula given in the literature.

$$P(\%) = \frac{m^1 - m^2}{m^1 - m^3} \quad (4)$$

Where m^1 is the sample weight before anodization, m^2 is the sample weight after anodization, and m^3 is the sample weight after removing the PS layer with 5% KOH solution for 60 seconds. Figure 7 illustrates the SEM image of the PS layer formed on the N-type c-Si (111) sample. The surface of the c-Si sample cracked, and pores were not evidently observed. The etched surface became rougher than the c-Si surface, indicating low porosity (approximately 14.5%). Figure 7 demonstrates the SEM image of the PS layer formed on the P-type c-Si (100) sample. Pores with sphere-like appearances and thick walls were evidently randomly distributed on the PS surface. A modest density of pores was observed, and porosity was approximately 45%, higher than the 27% porosity of the PS layer formed on the N-type c-Si (100) sample (Fig. 7). The surface of the c-Si sample cracked, and numerous new pores evidently formed inside the cracks. Additionally, the surface of the c-Si sample was completely etched and consisted of numerous

discrete pores that formed over the wall that did not crack, and the pore walls widened, reducing the number of pores on the PS surface. Hence, porosity decreased. The average pore diameter (d) for the PS layer formed on the N-type c-Si (100) wafers was 5.9 nm and calculated using equation (2) below [13]:

$$E(eV) = E_g + \frac{h^2}{8d^2}\left(\frac{1}{me^*} + \frac{1}{mh^*}\right) \quad (5)$$

where E (eV) is the energy band gap of the PS layer calculated from the PL peak. Eg is the energy band gap of bulk c-Si. h is Planck's constant $= 4.13 \times 10^{-15}\ eV.s$, where as Me* and Mh* are the electron and hole effective masses, respectively (at 300 K, Mh* $= 0.19m_0$, Me* $= 0.16m_0$, and m_0 = $9.109 \times 10^{-31}\ kg$). In single layered porous, only one layer with approximately equal porous distribution will be observed and the porosity of the layer depends on the solution concentration, current density, etching time and the doping of the substrate. Therefore, low solution concentration (i.e 10%), high current density (i.e 20 mA/cm²), longer anodization time (i.e 20 minutes) and low doped wafer were used and high porosity is observed which is suitable for solar application. For the multilayer porous, more porosity was observed because of the parameters used which favours high porosity since it has double layer each with suitable values for high porosity in the anodization process.

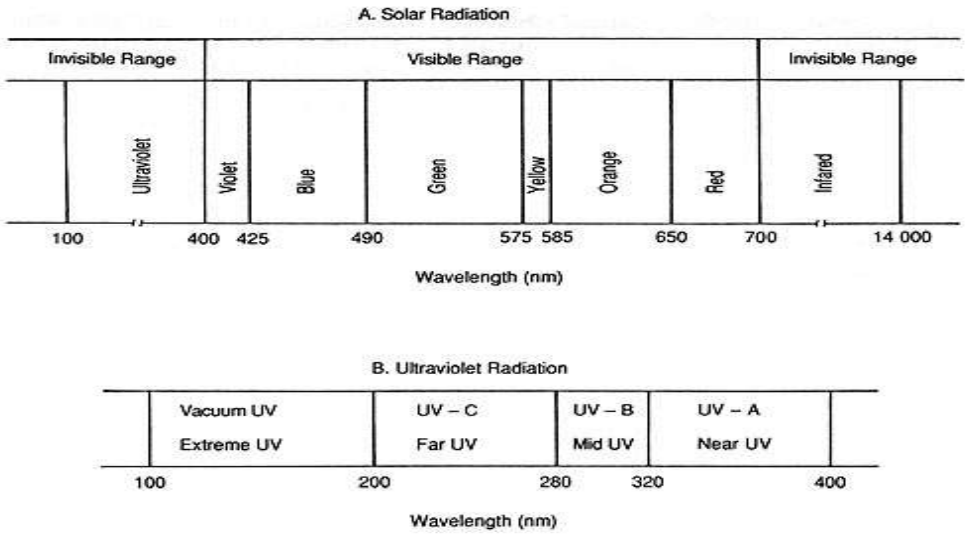


Figure 8: Solar spectrum

Figure 8 shows the solar spectrum with the wavelength of the solar radiation ranging from ultraviolet (UV) until infrared. The photovoltaic measurement (i.e microvolt against wavelength) done on the sample, it showed that there is an increase in the UV range compared to existing solar panel measured under same condition. The measurement starts from 200 nm until 1500 nm from which we observed shift on the prepared sample which start producing voltage from 200 nm while standard solar start from 300 nm as seen in figure 9.

Furthermore, there is an increase in the infrared region where the prepared samples end at 1500 nm while standard solar ends at 1100 nm. This resulted due to the hetero-junction existed between the crystal and the porous part of the silicon. This is because of the change in the Fermi energy, since Fermi energy level tries to be at a point where the charge carriers are equal both at valance and conduction band in a semiconductor, since the area where the silicon is etched, there will be a changed in the concentration of the charge carries, so the Fermi energy change in that particular position, but in the crystal part of the sample it remains where it is originally. The two Fermi energy of the porous and non-porous site tries to align themselves, but due to different in level the Fermi energy bends and more charge carries gather on that point which created a voltage at that position.

In general, for the whole spectrum the prepared sample produces high voltage compared to existing solar as we can see in figure 9. This is due to the accumulated charges on the porous side, since it's doped with different impurity (i.e N-impurity for p-substrate and vice versa), due to that a P-N junction is formed which consist of charges accumulated at the junction barrier. And as well the hetero-junction we have explained so far due to these two junctions the voltage will be higher compared to the other part of the substrate, therefore the voltages observed per each spectrum is higher in the sample than the standard solar due to this reason. Moreover, all the samples were measured and the spectrum is shown clearly that there is absorption from UV until infrared which showed that all the methods used are positively effective towards the efficiency of the sample (i.e crystalline silicon). Figure 10

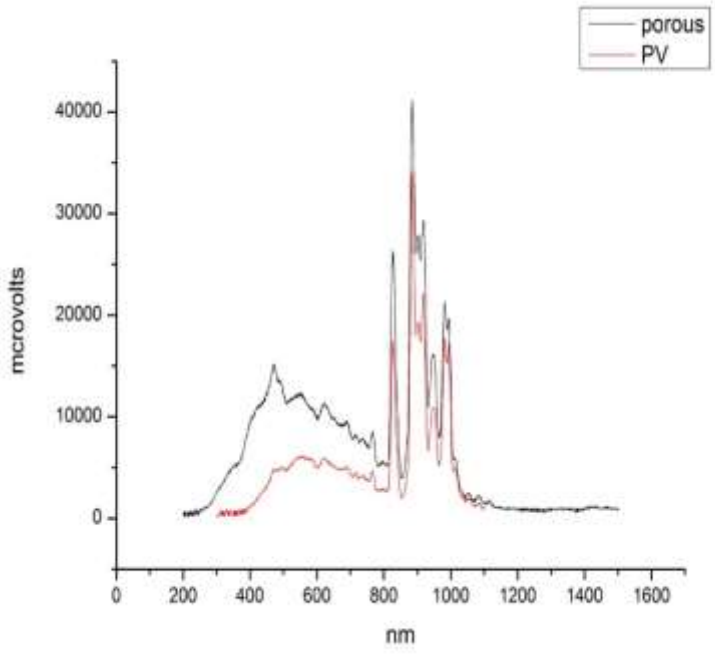


Figure 9. Photovoltaic measurement of standard solar (i.e red C) and fabricated solar (i.e black B)

Furthermore, from figure 7 we can see that almost all the spectrum is absorbed through the surface. This

was due to antireflection coating (ARC) of the porous layer. Because, now is a rough surface as a result of the etching, this layer played a vital role in the enhancement of quantum efficiency of a solar cell (i.e photo-conversion). This also increase the absorption in the visible region of the spectrum which is expected to increase the efficiency of the solar cells. The I-V measurement was done, the corresponding currents and voltages were recorded then later the power is obtained. Using these results, the curve was plotted as I-V curve and power curve were all plotted on same graph as seen in figure 10, the results are tabulated in table 1 as shown below. As shown in figure 10, the I-V curve of the sample is shown along with the power curve obtained from the voltages and the corresponding currents.

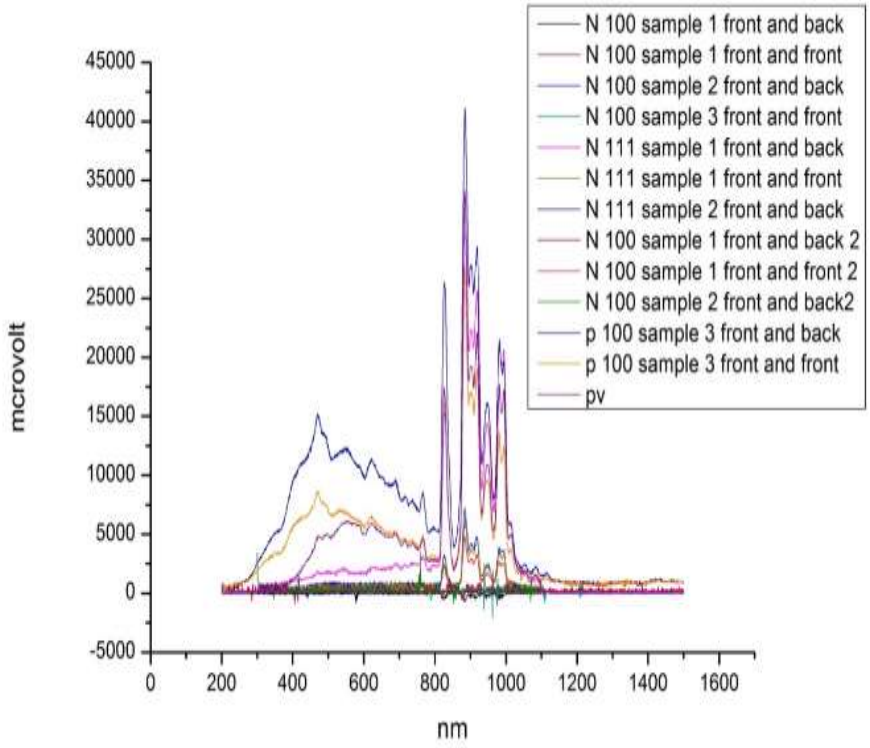


Figure 10. Photovoltaic measurement of all the prepared samples.

The maximum point of the power curve determines the point of maximum current (i.e. I_{max}) and point of maximum voltage (i.e. V_{max}) from which the efficiency can be calculated. The light source used has the illumination power on the sample as follows:
Power of the lamp = 120 W
Distance to the sample = 23 cm
The source will be considered as a point source so that the distance from the source to the sample to be the radius, any point from the source should be considered as a sphere; therefore, the area is given by:

Area = $4\pi r^2 = 4 \times \pi \times (23)^2 = 6648.472$ cm²
Now, the input power to the solar surface (P_{in}) = $(light\ power)/area$

P_{in} = 120/6648.472 W/cm²
P_{in} = 0.01804926 W/cm² ≈ 18.05 mW/cm²

Table 1. Current, voltage and power of the porous silicon obtained from the measurement.

Current (A)	Voltage (V)	Power (W)
0.0158	0.0000	0.0000
0.0158	0.0280	0.0004
0.0155	0.0730	0.0011
0.0152	0.1500	0.0023
0.0149	0.1720	0.0026
0.0146	0.1820	0.0027
0.0143	0.1910	0.0027
0.0140	0.1960	0.0027
0.0137	0.2030	0.0028
0.0134	0.2080	0.0028
0.0131	0.2120	0.0028
0.0128	0.2160	0.0028
0.0125	0.2200	0.0028
0.0122	0.2230	0.0027
0.0119	0.2260	0.0027
0.0116	0.2290	0.0027
0.0113	0.2320	0.0026
0.0110	0.2350	0.0026
0.0107	0.2360	0.0025
0.0104	0.2390	0.0025
0.0000	0.2780	0.0000

We have seen that the maximum current and maximum voltage are obtained from the maximum point of power, therefore these are obtained from figure 10 as;

$$I_{max} = 13.4\ mA/cm^2$$
$$V_{max} = 208\ mV$$

Therefore, the efficiency is given by;

$$\eta^p = I_{max} \times V_{max}/p_{in}$$

Where η^p = efficiency of the porous sample prepared.

$$\eta^p = {(13.4 \times 208 \times 10^6)}/{(18.05 \times 10^3)}$$

$\eta^p = (13.4 \text{ x } 208 \text{ x } 10^6)/(18.05 \text{ x } 10^3)$
$\eta^p = 0.1544$
$\eta^p = 15.44\ \%$

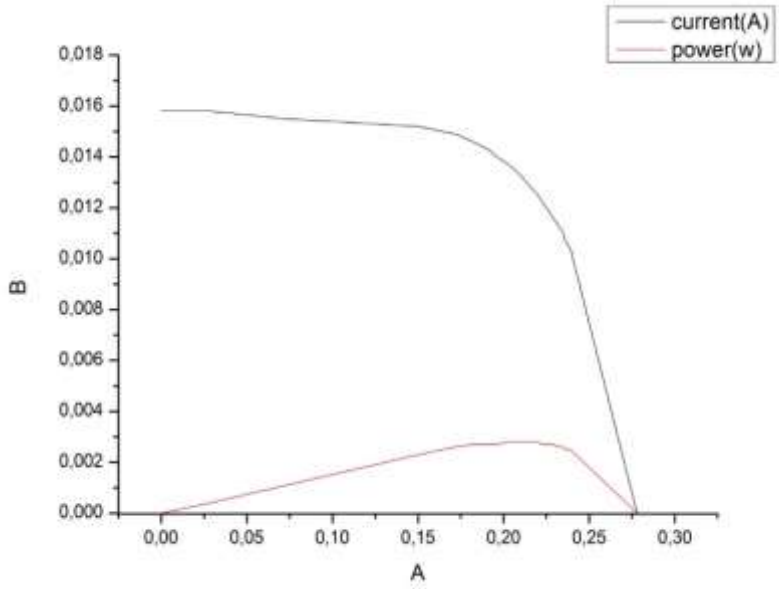


Figure 11. I-V curve and power curve on same graph, with 'B' equals to current in amperes/centimeter squares and 'A' equals to voltage in volts.

Now consider the non-etched c-silicon from which the above mention porous silicon is made and the efficiency found to be 15.44%, the I-V values are obtained using same method as the one used above (i.e. I-V measurement). The values were obtained as in table 2. The values show corresponding low voltage and low current compared to the prepared sample, which result in lower power and low efficiency as we can see below:

Already we knew the power of our illumination as obtained above, now we can see that the maximum voltage (V_{max}) and maximum current (I_{max}) that are corresponded with the maximum value of the power, we have:

I_{max} = 2.672 mA/cm² and V = 60.4090 mV,
and our P_{in} = 18.05 mW/cm²
Therefore, the efficiency is;
$\eta^n = (2.672 \text{ x } 60.4090 \text{ x } 10^6)/(18.05 \text{ x } 10^3)$,
where η^n = efficiency of the crystal silicon from which the sample is prepared (i.e. non-etched).
$\eta^n = 0.008725$
$\eta^n = 8.725\%$

Table 2. Current, voltage and power of the non-porous silicon obtained from the measurement.

Current (mA/cm²)	Voltage (mV)	Power (mW)
3.150	0	0
3.1500	16.7090	52.6334
3.0900	43.5650	134.6159
2.9710	49.9540	148.4133
2.9110	52.8580	153.8696
2.8510	55.4720	158.1507
2.7920	56.9240	158.9318
2.7320	58.9570	161.0705
2.6720	60.4090	161.4128
2.6120	61.5710	160.8235
2.5520	62.7330	160.0946
2.4930	63.8950	159.2902
2.4330	64.7660	157.5757
2.3730	65.6370	155.7566
2.3130	65.9000	152.4267
2.2540	66.7630	150.4838
2.1940	67.6260	148.3714
2.1340	67.9140	144.9285
2.0740	68.7770	142.6435
0.0000	80.0000	0.0000

If we compare the two efficiencies, it is clear that the porous sample has higher efficiency than the crystalline silicon. Therefore, we can see the enhancement by taking the differences between the two results which is;

$\eta_i =$ increase in efficiency by the method observed in this work,
$\eta_i = (\eta^p - \eta^n)$ %
$\eta_i =$ (15.44 - 8.725) % = 6.715%,

We can see from figure 9 the I-V curves varies for the non-etched and the etched sample which later have higher I-V curve indicating more efficiency compared with the former. More information can be obtained from figure 7 that shows the effect of the methods used on the c-silicon to enhance its efficiency. All the measurements were taken under same condition so that to realize the effect of what have been done to the wafer in order to manipulate the efficiency.

Throughout the study, some steps where repeated more than ones in order to get good result, because it is not easy to convert the design to the desired device, repeated trials must be done to obtain the approximate value in the design.

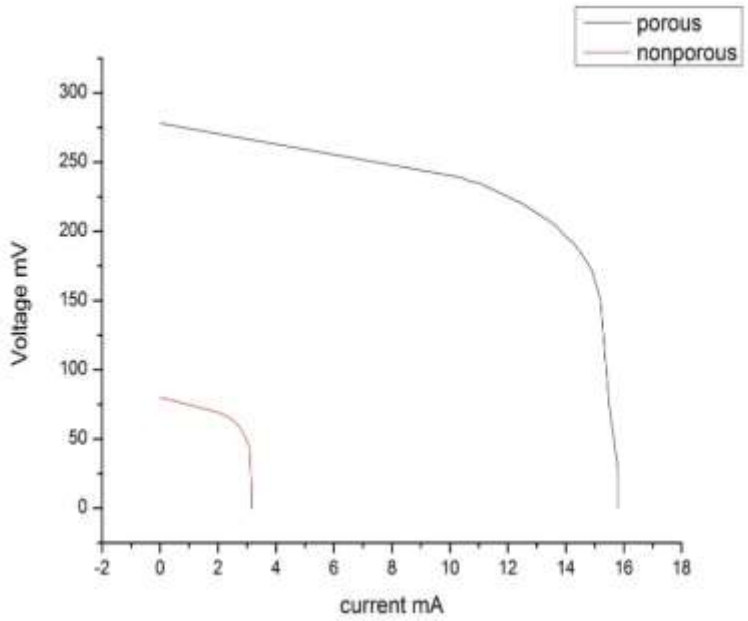


Figure 12. I-V curve of porous and non-porous in comparison.

4. CONCLUSION

Going by the discussion, it shows that by taking the previous steps mentioned in methodology of this work we can have enhanced the efficiency of crystalline silicon by approximately 6.715% which is significant in solar application. Moreover, the doping or amount of impurity in the crystalline silicon is also important; if we apply same method on the low resistive wafer, we can obtain higher efficiency though the enhancement is same (i.e. 6.715%). Furthermore, more absorption of solar spectrum can be observed using same method. These can be used in many applications that needs higher absorption of the spectrum.

ACKNOWLEDGEMENT

The authors are grateful to ***Prof. Dr. Bayram Unal*** of Istanbul University-Cerrahpasa, Istanbul, Turkey for his enormous contributions towards the success of the study and also acknowledge the staff of BioNano Technology Research and Development Center, Fatih University, Istanbul, Turkey for the constant and technical support during this research.

REFERENCES

[1] Hummelen, J. C., Shaheen, S. E., Brabec, C. J., Fromherz, T., Saricifici, N. S. and Padinger, F., (2001), "2.5% efficient organic plastic solar cells", Applied Physics Letters, Vol. 78, No. 6, pp. 841-843.

[2] Uhlir, A. and Uhlir, I., (2005), "Historical perspective on the discovery of porous silicon", Physica Status Solidi, Vol. 2, No. 9, pp. 3185-3187.

[3] Elisabet Xifré Pérez, Fundementals of porous silicon and applications, In: Design, Fabrication and Characterization of Porous Silicon Multilayer Optical Devices, Universitat Rovira I Virgili, ISBN: 978-84-691-0362-3/DL: T.2181-2007, pp. 5-26.

[4] Gutlich, P., Bill, E. and Trautwein, A. X., Mossbauer spectroscopy and transition metal chemistry:

Fundamentals and applications, first ed., Springer-Verlag Berlin Heidelberg, 2011.
[5] Dinu, N., Instrumentation on silicon detectors: from properties characterization to applications. Instrumentation and Detectors [physics.ins-det]. Université Paris Sud - Paris XI, 2013. fftel-00872318.
[6] Chanda, S. K., (2008), "Copper doped window layer for CdSe solar cells", Graduate Theses and Dissertations. https://scholarcommons.usf.edu/etd/168
[7] Fox, M. and Ispasoiu, R., (2017) Quantum Wells, Superlattices, and Band-Gap Engineering. In: Kasap S., Capper P. (eds) Springer Handbook of Electronic and Photonic Materials. Springer Handbooks. Springer, Cham.
[8] Ananda, W., (2017), External quantum efficiency measurement of solar cell, 15th International Conference on Quality in Research (QiR): International Symposium on Electrical and Computer Engineering, pp. 450-456. https://doi.org/10.1109/QIR.2017.8168528
[9] Kanevce, A., Reese, M. O., Barnes, T. M., Jensen, S. A. and Metzger, W. K., (2017), "The roles of carrier concentration and interface, bulk, and grain-boundary recombination for 25% efficient CdTe solar cells", Journal of Applied Physics, Vol. 121, No. 21. https://doi.org/10.1063/1.4984320
[10] Energy efficiency: The elusive negawatt. https://www.economist.com/briefing/2008/05/08/the-elusive-negawatt, 2008 (accessed 21.08.2013).
[11] Almosni, S., Delamarre, A., Jehl, Z., et al., (2018), "Material challenges for solar cells in the twenty-first century: directions in emerging technologies", Science and Technology of Advanced Materials, Vol. 19, No. 1, pp. 336–369. https://doi.org/10.1080/14686996.2018.1433439
[12] Ossicini, S., Pavesi, L. and Priolo, F., Light emitting silicon for microphotonics, first ed., Springer-Verlag Berlin Heidelberg, 2003. https://doi.org/10.1007/b13588
[13] Cullis, A., Canham, L. and Calcott, P. D. J., (1997), "The structural and luminescence properties of porous silicon", Journal of Applied Physics, Vol. 82, No. 3, pp. 909-965. https://doi.org/10.1063/1.366536